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(54) INSULATED GATE SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

(57) Abstract:

PROBLEM TO BE SOLVED: To maintain the high withstand voltage of a device by forming a third semiconductor layer that is deeper than the second semiconductor layer at direct under gate wiring.

SOLUTION: A p semiconductor layer 13 is foamed being connected to and surrounding a p base layer 4 that is formed on a cell region CR in which gate electrodes 10 are arranged. An emitter electrode 11 is connected to the upper surface of the side diffusion region SD of the p semiconductor layer 13 and to the upper surface of a margin region MR that is adjacent to the side diffusion region SD through a contact hole CH. An n^+ layer 5 is not formed in these regions. Most of avalanche holes H that are generated around the side diffusion region SD when high voltage is applied to it go through the side diffusion region SD and a part of it go through the margin region MR and then are exhausted to the emitter electrode 11. As there exists no n^+ emitter layer 5 in these route, no parasitic bipolar transistor is conducted by the passage of holes H. As the result of it, reverse biased safely operating region characteristic is improved.